COMP4300 Spring 2019

Homework 2

1. Suppose you are designing a cache for a machine with 40-bit addresses. The cache is 1MB in size. Cache blocks are 64 bytes.

1MB = 1,048,576 bytes

* 1. How many blocks can be held in the cache?

1,048,576 / 64 = 16,384

16,384 blocks = 214

* 1. How many bits of the address are devoted to the offset?

64 bytes per block, log2(64) = 6

6-bit offset

* 1. If the cache is direct-mapped, how many bits are devoted to the tag and index?

log2(16,384) = 14, 40-6-14 = 20

20-bit tag, 14-bit index

* 1. If the cache is 4-way set associative, how many bits are devoted to the tag and index? How many sets are there?

16384 / 4 = 4096, log2(4096) = 12, 40-6-12 = 22

22-bit tag, 12-bit index, 4096 sets

* 1. If the cache is fully associative, how many bits are devoted to the tag and index?

40-6 = 34

34-bit tag, 0-bit index

1. Suppose you have a machine with separate I- and D- caches. The miss rate on the I-cache is 2%, and on the D-cache 3%. On an I-cache hit, the value can be read in the same cycle the data is requested. On a D-cache hit, one additional cycle is required to read the value. The miss penalty is 100 cycles for either cache. 35% of the instructions on this RISC machine are LW or SW instructions, the only instructions that access data memory. A cycle is 2ns. What is the average memory access time?

MRI = .02 MRD = .03 MP = 100cycles LW/SW = .35instr CT = 2ns